An Integrated Circuit Transformer For Radio Frequency Applications

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Background of Invention

The present invention relates to microwave components used in radio and telephone communications. Specifically, an integrated circuit transformer is disclosed which can be used as a multi-winding balun transformer in radio frequency applications.

SiGe integrated technology has been used to manufacture integrated circuits to implement RF receivers as well as RF transmitters in wireless personal communications systems. Radio frequency signal circuits typically require inductances or transformers having multiple windings to perform standard radio frequency circuit functions. Wireless telephones, for instance, require receivers which have tuned circuit inductors and transformers in the first RF section, and have mixer circuits which use transformers for converting the received microwave signals into intermediate frequency signals. Compared to other passive circuit components, the integration of inductances and transformer elements for performing these functions is considerably more difficult in VLSI technology. Specifically, whereas micro-strip components may be used to create inductances and transformer windings, attempts to integrate them in VLSI technology has been limited by the high losses that substrate dielectrics present to a micro-strip component.

Attempts have been made to implement a transformer windings in multi-layer metallization surfaces separated by a silicon oxide insulation layer. These attempts, however, have been unsuccessful in controlling the high parasitic capacitance which occurs between windings on different metallization layers of a VLSI circuit. The high parasitic capacitance is especially troublesome when using a transformer in a differential mode application since the parasitic capacitance

degrades common mode rejection which is desired in circuits which are intended to operate in a differential mode.

The present invention is directed to improvements in transformer designs for such VLSI applications.

Summary of the Invention

An integrated circuit transformer is formed on a substrate having multiple metallization layers separated by an insulation layer. A primary winding of the transformer includes winding turns on each of two metallization layers separated by the insulation. A secondary windings for the transformer may be formed on either metallization layer, and each of the turns of the secondary winding are separated by a turn of the primary winding.

In one embodiment of the invention a balun transformer is provided. Secondary windings are included on both metallization layers bearing a portion of the primary winding. The transformer exhibits parasitic capacitance only between turns of the primary winding which are on different metallization layers, and not between turns of the primary and secondary winding which are on the same metallization layer, thus preserving the common mode rejection for the transformer.

Description of the Figures

Figure 1A is a conventional planar transformer of the prior art.

Figure 1B is the lumped equivalent circuit for the transformer of Figure 1A.

Figure 2A illustrates the parasitic capacitance which degrades common mode rejection when primary and secondary windings are on different metallization layers of an integrated circuit.

Figure 2B illustrates the equivalent circuit for the transformer of Figure 2A.

Figure 3A is a schematic representation of a primary and secondary winding of a transformer in accordance with a first embodiment of the invention.

Figure 3B illustrates the lumped equivalent circuit of the transformer of Figure 3A.

Figure 4A illustrates the primary winding of a transformer in accordance with a second embodiment of the invention.

Figure 4B illustrates secondary windings of a transformer in accordance with the second embodiment of the invention.

Figure 4C illustrates a three dimensional representation of the primary winding and secondary windings of the second embodiment of the invention.

Figure 5A illustrated the process step of forming a first metallization layer over semiconductor devices formed in a substrate.

Figure 5B illustrates the process of forming a first winding segment for a primary winding of the transformer with an interleaved secondary winding.

Figure 5C illustrates the process of forming a second insulation layer over the first metallization layer for supporting a second primary winding segment and a second secondary winding.

Figure 5D illustrates the process of forming the second segment of the primary winding and the second secondary winding.

Description of the Preferred Embodiment

Referring now to Figures 1A and 1B, there is shown, respectively, a conventional balun transformer wherein a first primary winding 1-2 is co-planer with a secondary winding 3-4, and its lumped equivalent circuit . The resulting transformer has the known relationship defining mutual coupling K described as follows:

$$K=M/(L1 \times L2)^{1/2}$$

The impedance ZIN looking into the transformer primary winding 1-2 terminals is proportional to the load impedance ZL connected to the terminals of secondary winding 3-4 as:

$$ZIN = ZL \times (L1/L2)$$

When the transformer is implemented in VLSI, it occupies significant substrate area. To reduce the substrate area occupied by the transformer, a stacked winding as shown in Figure 2A has been attempted. The primary winding 1-2 and the secondary winding 3-4 exist on separate metallization layers of a substrate separated by a dielectric such as silicon oxide. In many applications for personal wireless communications systems, a balun transformer provides differential mode signal processing where high common mode rejection is desirable. The lumped equivalent circuit for the circuit of Figure 2A is represented by Figure 2B which illustrates the problem of parasitic capacitance Cp between primary windings 1-2 and secondary windings 3-4 which reduces the circuit Q for the device and degrades balun transformer common mode rejection.

The first embodiment of the invention is represented schematically in Figure 3A, and its lumped constant equivalent circuit is shown in Figure 3B. In accordance with the present invention, multiple metallization layers 8,9 are provided on a substrate for forming the turns of the primary winding 1-2 and a secondary winding 3-4. As shown in Figure 3A, the primary winding 1-2 has first and second segments 10,11 occupying different metallization layers 8,9 of the VLSI circuit. The primary winding segments 10,11 are connected through a circuit via 12 in an insulating layer separating the metallization layers 8,9. A single secondary winding 3-4 is shown on one metallization layer 8 only, each turn of which is separated by a turn of the primary winding segment 11 on the same metallization layer 8 and coplanar therewith. As illustrated in the equivalent circuit of Figure 3B, the parasitic capacitance Cp is confined to turns of different segments 10,11 of the primary winding 1-2, and does not occur between the primary winding 1-2 and secondary winding 3-4. Accordingly, improved common

mode rejection results since the parasitic coupling between primary and secondary has been significantly reduced over that of Figure 2A.

By providing one segment 11 of the primary winding 1-2 on one layer, and the second segment 10 on another layer 9, separated by a dielectric such as SiO2, it is possible for a given area of the substrate supporting the multiple layers to have a winding with increased inductance (or, conversely, using less substrate area to achieve the same inductance), since the inductance increases as the square of the number of turns. Accordingly, more turns for each winding are possible using the stacked structure according to Figure 3A for a given surface area then that of Figure 1A of the prior art where both primary 1-2 and secondary 3-4 windings have to be provided on a single layer.

Figures 4A, 4B and 4C represent a particular type of compact multi-level transformer which is useful in applications such as a doubly balanced mixer. The primary winding shown in Figure 4A has ends 13 and 14 which are connected to turns of different segments 15, 16 of the primary winding which are on different metallization layers. The segments are connected to each other through a via 17 constituting a vertically extending conductor. The secondary windings 18, 21 shown in Figure 4B have ends 19, 20, 22 and 23 respectively. Each of the secondary windings 18, 21 is located on the different metallization layers 25, 26 of Figure 4C, and are wound concentric with the segments 15, 16 of the primary windings on each of the metallization layers 25, 26. Each turn of the secondary windings 18, 21 is separated from an adjacent turn by a turn of the primary winding segment 15, 16 on the respective metallization layer 25, 26.

Referring to Figure 5A, the process of implementing transformers in accordance with the foregoing begins with a substrate 29 having silicon devices 30 which form the active circuit devices. Once the active circuit areas are formed, a silicon dioxide (SiO2) insulating layer 31 is applied to the active silicon area of the chip and the first metallization layer 32 is deposited on the insulating layer 31. Following the step of metallizing the insulation layer, the turns of a segment of the

primary winding 34, along with the turns of a secondary winding 35 are formed as an interleaved pattern on the metallization layer using photolithography as shown in Figure 5B. Once the secondary and primary windings 34, 35 have been patterned and etched in the interleaved pattern so that the turns of each winding are separated by turns of the other winding, a second insulation layer 36 is applied as shown in Figure 5C. Figure 5D shows a top metallization layer for forming the turns of the remaining segment of the primary winding 34 formed on the insulation layer 36. Using photolithography, the top primary winding segment 38 is patterned and etched along with the secondary winding 39 as was done with the previous metallization layer. A via 40 is formed through the insulation layer 36, and a vertical conductor is established to connect the ends of the primary winding segments 34,38 with a vertical conductor as shown.

A third metallization layer (not shown) may be formed over a subsequent insulation layer 37 to provide exit connections for the transformer winding ends.

Thus, there has been described with respect to the several embodiments of the invention, a multi-level transformer and process for making thereof. The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention in the context of a voltage controlled oscillator, but, as mentioned above, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings and/or the skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to

the form or application disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.